

REMARKS

Paragraph 57 of the specification has been amended to provide that related U.S. patent application 10/780,030 has issued into U.S. Patent 6,975,544 B2.

Entry of the present amendment will not entail materially added work on the Examiner's part. No more than a cursory review of the record will be needed. Accordingly, this amendment should be entered.

Please telephone Attorney for Applicant(s) at 650-964-9767 if there are any questions.

**EXPRESS MAIL LABEL NO.:**

**EV 743 585 224 US**

Respectfully submitted, . . .

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application No.: 10/780,031 Confirmation No.: 9275  
First Named Inventor: Park, Jongmin Filing Date: 17 February 2004  
Group Art Unit: 2824 Examiner: Wendler, Eric J.  
Atty. Docket No.: R-0003 US  
Title: Technique for Programming Floating-gate Transistor Used in  
Circuitry Such as Flash EPROM  
Assignee(s): ProMOS Technologies Inc.

Mountain View, California  
18 July 2006

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**AMENDMENT TO DRAWINGS UNDER 37 CFR 1.312**

Sir:

Responsive to the Notice of Allowance mailed 19 April 2006 and under the provisions of 37 CFR 1.312, the drawings of the above patent application should be amended in the following manner.

In Fig. 3, label "p" should be added to region BR.

In Fig. 4, an arrowhead should be added to the lead line for reference symbol " $V_{DD}$ " near the middle of the figure; and a short horizontal line should be added along the vertical axis next to reference symbol " $V_{SPH}$ " at the height of the label " $V_{SPH} \approx 6 V$ ".

In Fig. 15, reference symbol "GD" should be added to the thick-line diagonally shaded region directly below region FG.

Enclosed is a copy of the relevant drawing sheets in which the foregoing changes are indicated in red.

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## REMARKS

Applicant's has requested that the drawings be revised to correct several self-evident errors. In particular, Applicant's Attorney has requested that:

- a. The label "p" be added to p-type region BR in Fig. 3 in conformity with how p-type region BR is labeled "p" in Fig. 15;
- b. An arrowhead be added to the lead line for reference symbol " $V_{DD}$ " near the middle of Fig. 4 in conformity with how the lead lines for reference symbols " $V_{CPH}$ ", " $V_{SPH}$ ", and " $V_{ITM}$ " in Fig. 4 all have arrowheads;
- c. A short horizontal line be added to Fig. 4 along the vertical axis next to voltage reference symbol " $V_{SPH}$ " at the height of the label " $V_{SPH} \approx 6 \text{ V}$ " in conformity with how the other voltage levels along the vertical axis are marked with short horizontal lines; and
- d. Reference symbol "GD" be added to the thick-line diagonally shaded region directly below region FG in Fig. 15 in conformity with how the thick-line diagonally shaded region directly below region FG in Fig. 3 is labeled "GD".

Entry of the present amendment will not entail materially added work on the Examiner's part. No more than a cursory review of the record will be needed. Accordingly, this amendment should be entered.

Please telephone Attorney for Applicant(s) at 650-964-9767 if there are any questions.

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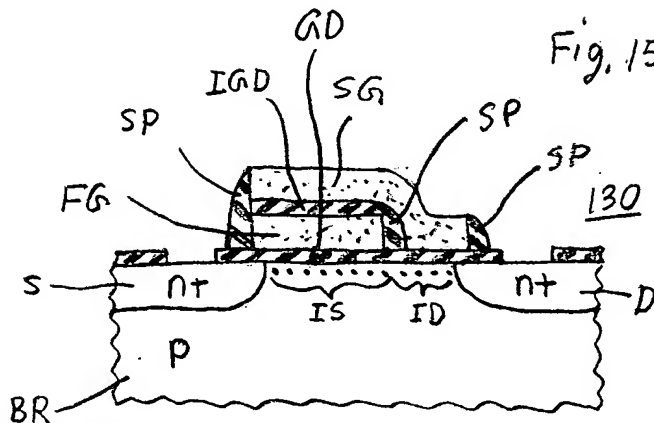
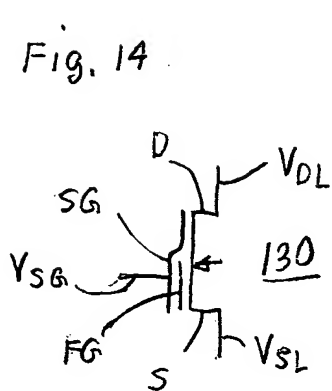
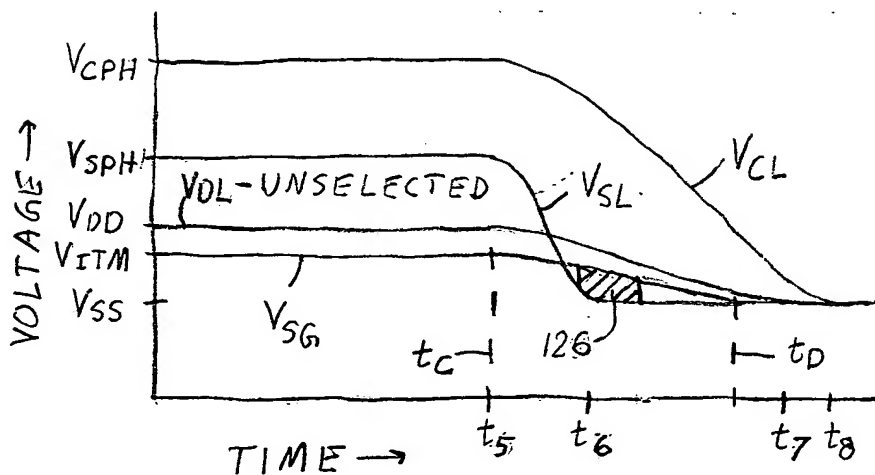
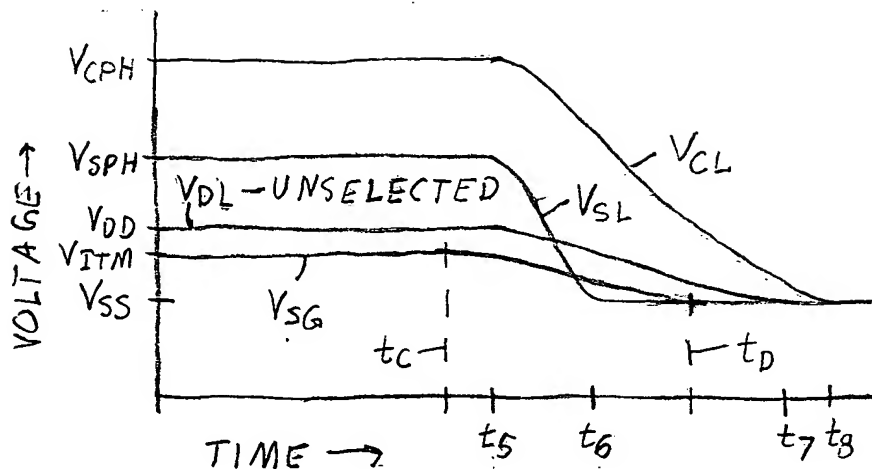
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A cross-sectional diagram of a semiconductor device. The structure consists of several layers and regions. At the base is a layer labeled 'BR'. Above it is a layer labeled 'P'. On top of the 'P' layer are two regions labeled 'n+' separated by a central region labeled 'IS'. Above the 'n+' regions are two regions labeled 'ID'. The top surface is covered by a layer labeled 'S'. Various other regions and structures are labeled: 'CG' (Control Gate), 'GD' (Gate Dielectric), 'IGD' (Inter-Gate Dielectric), 'SG' (Source Gate), 'SP' (Source Pad), 'FG' (Field Gate), and 'D' (Drain). The diagram shows a complex arrangement of these layers and regions, with some areas having different hatching patterns to indicate different materials or regions.

Fig. 4

